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December 31, 1991

Dr. Erhard Schimitschek, Scientific Officer
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Re:	Contractor	:	Northeast Semiconductor, Inc.
	Address	:	767 Warren Road, Ithaca, NY 14850
	Req. No.	:	s405811srv02/17 APR
	Contract No.	:	N00014-91-C-0222
	Report Date	:	December 31, 1991
	Report Title	:	Second Monthly Technical Report
	Period Covered	:	12/01/91 through 12/31/91

Dear Dr. Schimitschek:

Northeast Semiconductor, Inc. encloses its Second Monthly Technical (Line Item #0002) pursuant to the provisions of contract Section B entitled, "Supplies or Services and Prices/Costs" for the period of December 1, 1991 through December 31, 1991.

Innovative Techniques for the Production of Low Cost 2D Laser Diode Arrays

1.0 OBJECTIVE

The primary objective of this program is to develop a low cost, high yielding methodology for processing, packaging and characterization of MBE grown two dimensional high power laser diode arrays. Projected increases in overall yield of AlGaAs diode lasers would reduce manufacturing cost from the current $10 to $20 per peak watt to below $3 per peak watt. Emphasis will be placed on innovative packaging techniques that will utilize recent advances in diamond heat sinking technology.

2.0 PROGRAM METHOD AND SCHEDULE

This program consists of four phases which will demonstrate reduced manufacturing cost and improved device performance of NSI's MBE laser diode arrays. The four phases listed below will result in milestones in processing, packaging, and testing along with delivery of the specified number of 5-bar laser arrays.

(i) Concept phase: Conceptual design and organization of this phase II program. NSI will utilize the current side cooled strained relief package to manufacture 5-bar laser diode arrays for base line evaluation. (Deliverables: 3 5-bar arrays.)

(ii) Backplane phase: Development of a copper backplane cooling technology that incorporates CVD diamond submounts. This phase will also include the completion of room temperature photoluminescence development. (Deliverables: 5 5-bar arrays.)

(iii) Diamond Backplane phase: Develop a CVD diamond backplane cooling scheme that will utilize smaller CVD submounts. The reduction in submount size is to decrease the thermal resistance from the laser bar to the backplane. (Deliverables: 5 5-bar arrays.)

(iv) Liquid Cooled Submount phase: An innovative liquid cooled package will be developed. The CVD diamond submounts will be hermetically sealed, electrically isolated and liquid cooled. (Deliverables: 5 5-bar arrays.)

The following global issues not mentioned above will be investigated continuously throughout all four phases of this program:

(1) design and development of a mask set to increase processing and packaging yields,

(2) development and updating of MBE growth software,

(3) design and development of an in-house facet coating station,

(4) evaluation of different facet coating materials,

(5) development of automated tests,

(6) life test and burn-in development.

The master schedule for this program is shown in Table 1. Each phase will require wafer growth, processing, assembly and test. The schedule shows the estimated number of sample fabrications and tests, as well as the time of hardware deliverables and reports.

3.0 PROGRESS THIS PERIOD

3.1 Wafer Growths

The month of December marked a change in our approach to laser wafer growth in order to improve yield, uniformity, and performance. We have initiated a more rigorous approach to machine qualification after up-to-air episodes. This includes an improved vacuum system bake procedure, in which the substrate heater is outgassed to temperatures higher than those seen by wafers during laser growth. This procedure facilitates the removal of carbon monoxide and other residual gases from the substrate heater and its surroundings, lessening the chance of incorporating these background impurities later, during growth of product structures. The source material effusion cells are also elevated in temperature during the bake to remove background impurities. In a big departure from previous practice, these cells are not allowed to cool after the bake, and thus are prevented from becoming thermal sinks capable of re-absorbing residual impurities.

The above changes in procedure are expected to benefit the yield and performance of our opto-electronic materials. In the short term, however, we have experienced increased down time due to the failure of marginal equipment. The increase in environmental stress imposed on the vacuum system appears to have contributed to the failure of equipment near the end of its expected service life, and has also pointed out design flaws in newer parts. We are replacing failed parts with new or refurbished ones, and are working with MBE equipment vendors to obtain equipment better suited to our needs.

Repairs and upgrades of the MBE machines have not finished as of the end of 1991, and will continue during the first quarter of 1992. However, we have reached an operational level of machine performance and expect to resume the growth and shipment of laser wafers around the third week of January 1992.

3.2 Processing

The current facet coating experiment uncovered several unexpected problems. In all three runs, the coatings were non-uniform on both the front and rear facets contributing to poor performance. Initially, it was believed that the non-uniformity was caused by foreign particles (dust) present during the stacking of the diode bars in the jig. Further examination indicates that the laser diode bars and spacer bars (between each diode bar) are not cleaving along one crystal plane. Massive crystal plane jumping, along with dust particles, causes the stack to twist and become misaligned. This results in "shadowing" of the facets, which produces thinning and non-uniform coatings. Figure #1 is a

PIV plot of a laser diode mounted backwards. The 14 Watts of light is being emitted out of the rear facet of the laser diode. At this output, the rear facet reflectance is calculated to be approximately 65%, not the 97% expected.

Figure #2 shows the life test data of two arrays with TiO_2 as a front facet coating. The array in the nitrogen ambient lived longer than the array in air. Additional data is being gathered to thoroughly characterize the facet coatings.

Design of the new mask set is complete, and it is currently out for quotation. This mask set will increase yield by reducing current leakage sites and suppling test bars for pre-package screening.

3.3 Testing

Progress has been made in the development of a multi-array life test station. The goals to be met include simultaneously measuring power, voltage drop, and time intervals of 10 laser diode arrays. Presently, 5 stations with cooling stages, and the signal multiplexer are complete. Life test capability is currently limited by the number of pulsers available. Figure #3 is a schematic diagram of the proposed pulser. The PC board is under design and should be complete by the end of January. Software code is continuously developing as the need for increased capability, flexibility, and reliability grow.

3.4 Assembly and Packaging

Efforts continue this period on increasing packaging yield through improvements to the solder joint. Experiments with 100% In solder indicate that a thickness between 5 µm and 6 µm provides the optimal solder joint. To reduce absorption of the Au by the In and increase the strength of the joint, the amount of Au plated onto the copper submounts was reduced by a factor of 8. The single bar packaging yield for the month of December ended up at 93% (39 out of 42).

Evaluation began on the metalization of CVD diamond. The metalization scheme consists of 1000 Å Ti/2000 Å Pt/3000 Å Au. Samples were tested CW and the results are shown in Figure #4. The resistance measured is an order of magnitude higher than that expected and not acceptable for bar packaging. Additional pieces are being sent by the vendor with the same metalization for evaluation. In addition, we are investigating the feasibility of a multiple layer consisting of 1000 Å Ti/2000 Å Pt/20000 Å Au/1000 Å Ti and <1000 Å Au. The additional barrier of Ti and the flash of Au are needed to maintain a 12:1 In/Au ratio at the top layer. A possible replacement of the thick 20000 Å Au layer by Ag or Cu is also being considered.

4.0 PLANS FOR JANUARY

For the month of January, NSI plans to start development of backplane cooling technology. Investigation will continue on facet coatings, PL correlation to device performance, and CVD diamond. All global issues mentioned in Section 2.0 will be addresses and continuously investigated during this program.

Very truly yours,

Michael J. Cook,
Principal Investigator
Northeast Semiconductor, Inc.

MJC:nd
Encl: 1 Copy of 2nd Monthly Technical Report

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Statement A per telecon
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NWW 1/21/92

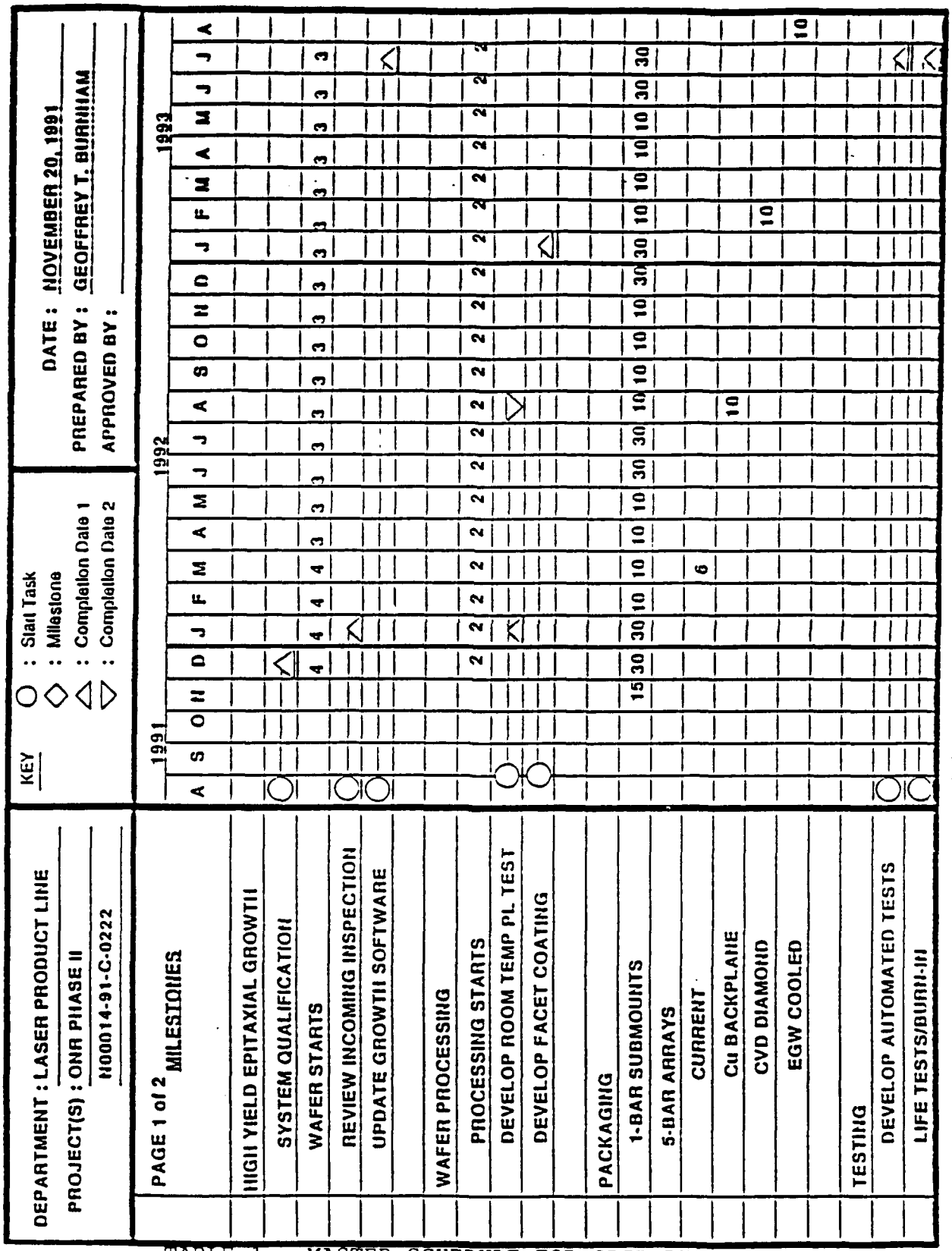


TABLE 1. MASTER SCHEDULE FOR SBIR PHASE I
CONTRACT NO. N00014-91-C-0222

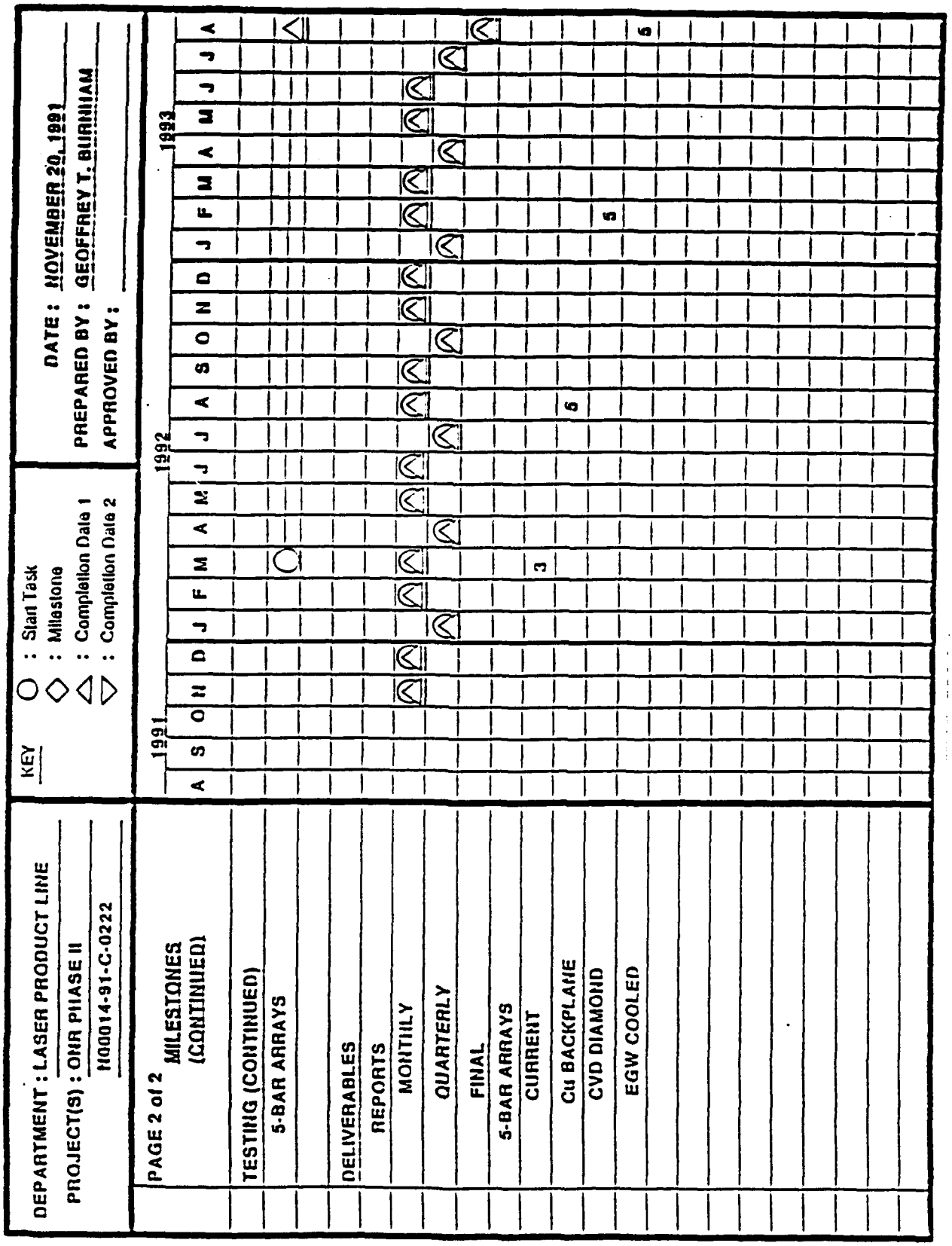


TABLE 1. MASTER SCHEDULE FOR SBIR PHASE I
(continued)

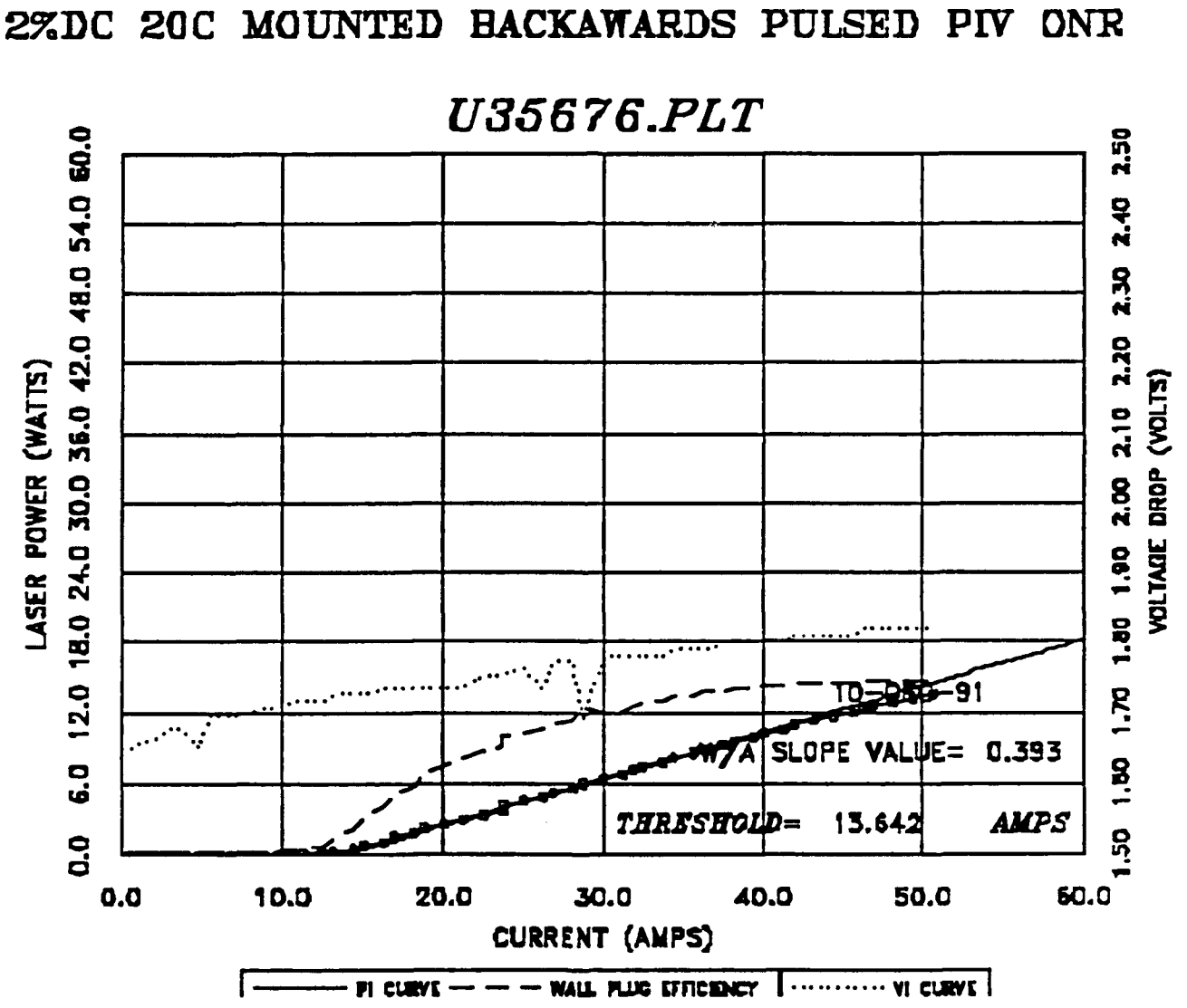
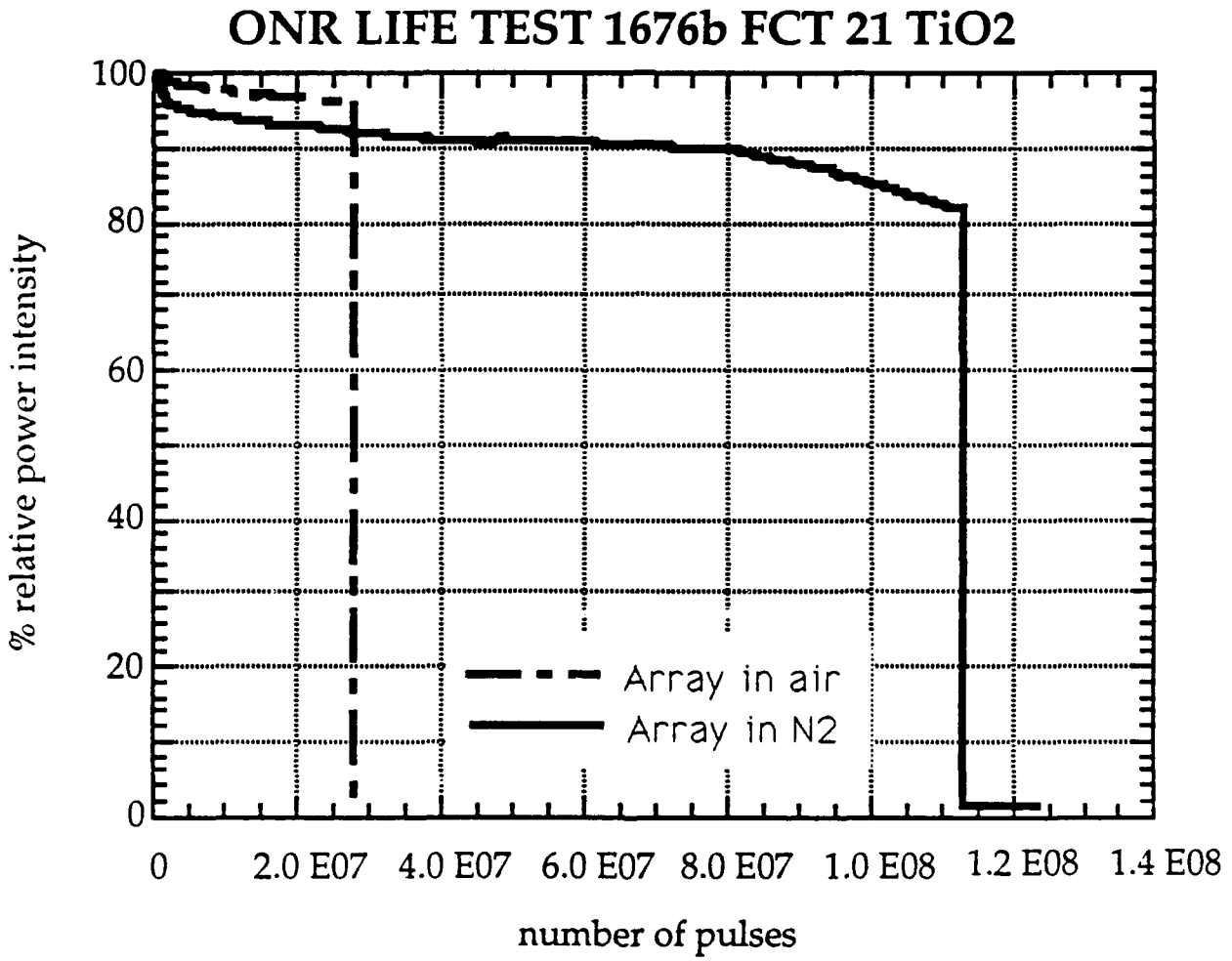


FIGURE 1. LASER DIODE ARRAY MOUNTED BACKWARDS



Operating conditions:
Duty cylce: 2.0%
Current: 50 Amps
Temperature: 20°C

FIGURE 2. LIFE TEST DATA

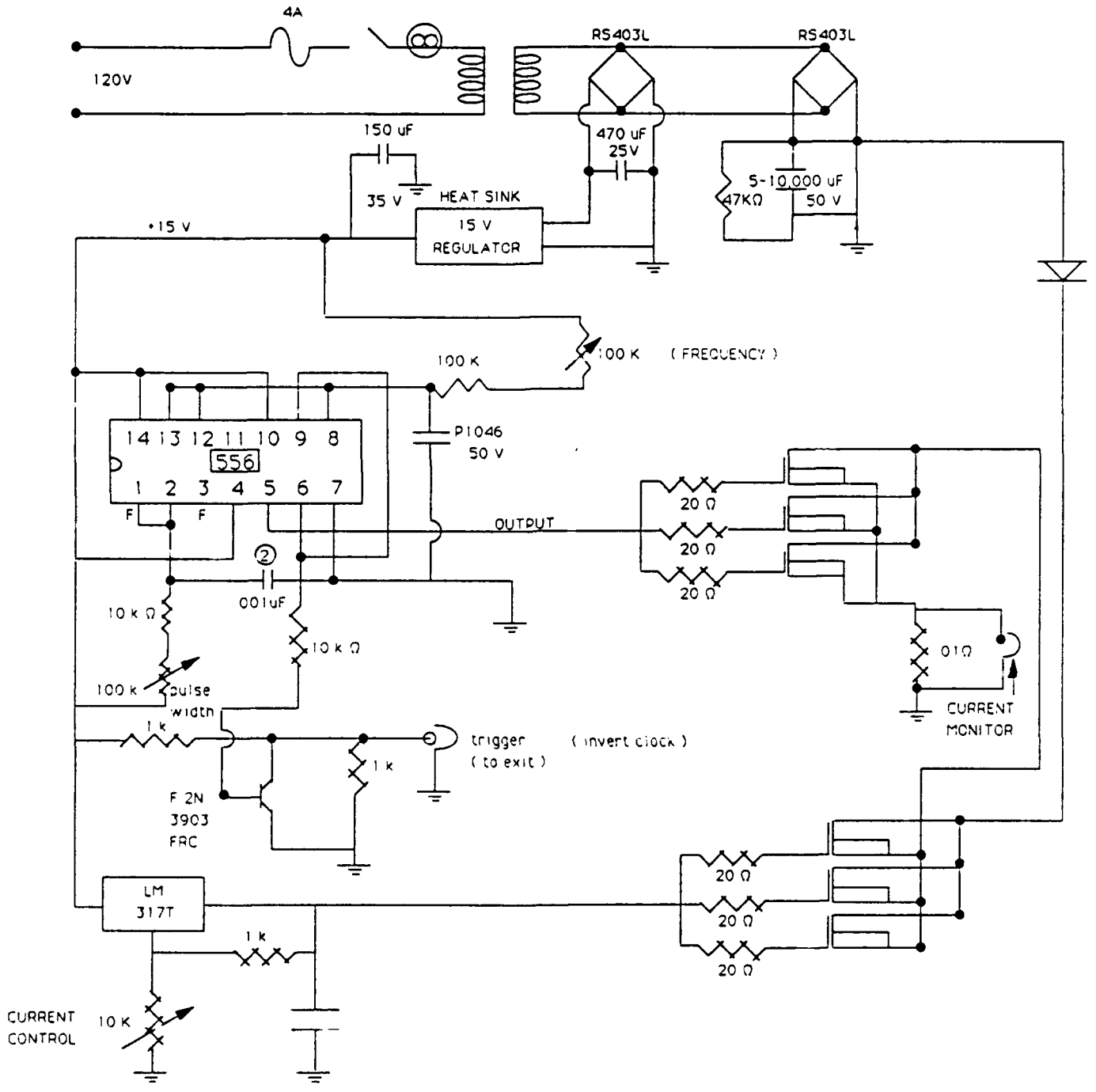
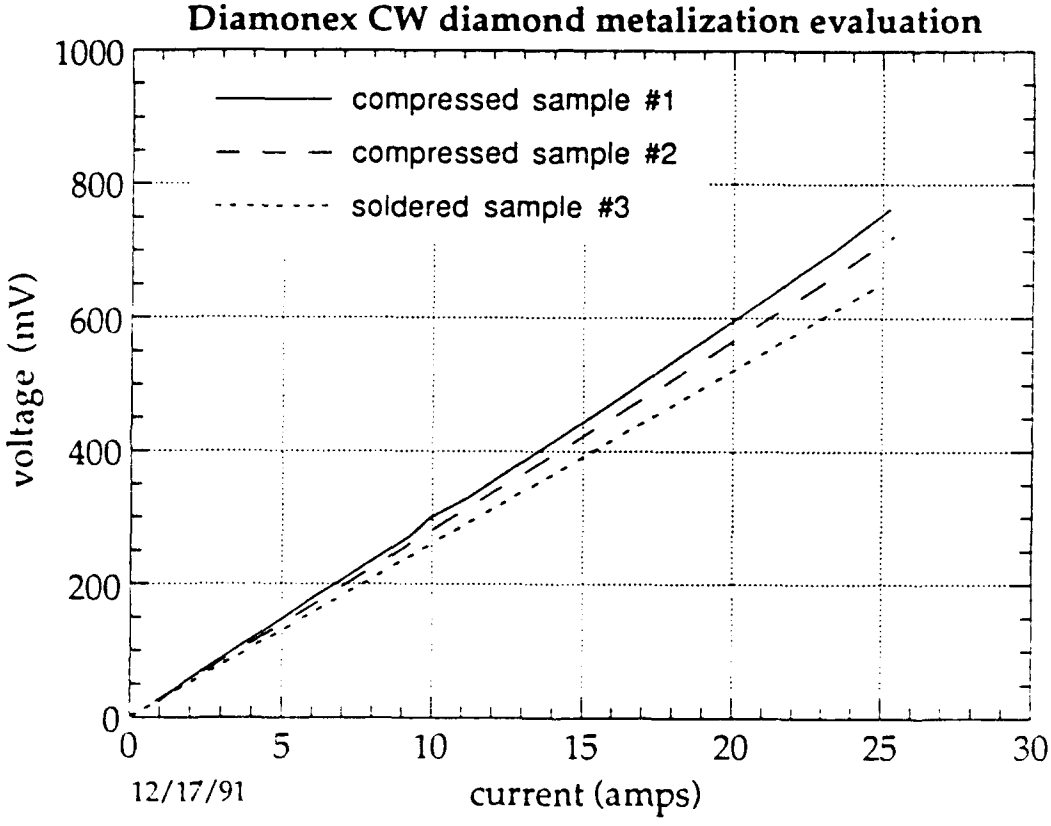


FIGURE 3. SCHEMATIC OF PULSER



Compressed Sample 1: resistance = 0.0300 Ω
Compressed Sample 2: resistance = 0.0284 Ω
Soldered Sample 3: resistance = 0.0261 Ω

FIGURE 4. CVD DIAMOND EVALUATION